REMARKS

Claims 1-10 are present for examination.

DRAWINGS

The Examiner is requested to approve the drawings previously submitted in which Figures 7-8 and 9-15 were labeled as prior art. Formal drawings were submitted in the amendment filed June 17, 2003

PRIOR ART REJECTION

Claims 1-10 stand rejected under 35 USC 103(a) as being unpatentable over applicant's admitted prior art (APA) in view of Bacerra (5,710,689).

The Examiner indicates that all elements of applicant's claims are shown in applicant's admitted prior art except for the first conductivity type well which is under the first source diffusion layer and at least partially underlies the element isolation film and having a lower dopant concentration than the first diffusion layer.

The Examiner's rejections are respectfully traversed.

Becerra teaches in Fig. 4 a first conductive type well (n-well) located under the first source diffusion layer (n+ source region) and at least partially underlying the element isolation film (FOX region), and having a lower dopant concentration than the first source diffusion layer (n+ source region), wherein the bottom of the first conductive type well (n-well) is at the same depth as the bottom of the second conduction type well (p-well) or at a level deeper than the bottom of the second conduction type well (p-well).

In addition, the first conductive type well (n-well) is electrically connected directly with the first drain diffusion layer (n+ drain region) but is never electrically connected directly with the first source diffusion layer (n+ source region), which structure is necessary to form the internal circuit composed of N/p/N parasitic bipolar transistor 16, n/p/N parasitic bipolar transistor 12, and two resistances 15 & 17 as illustrated in Fig. 4. If the first conductive type well (n-well) were electrically connected directly with the first source

diffusion layer (n+ source region) as well as with the first drain diffusion layer (n+ drain region), the first source diffusion layer (n+ source region) and the first drain diffusion layer (n+ drain region) would be electrically connected via by-pass of the first conductive type well (n-well). Thus, Becerra does not teach the first conductive type well (n-well) being located under the first source diffusion layer (n+ source region) and thereby being electrically connected directly with the first source diffusion layer (n+ source region).

In contrast, the input protection circuit of the present claims uses a first conductive type well 1a with lower dopant concentration than the source diffusion layer 3c is formed directly under the source diffusion layer 3c and thereby the first conductive type well 1a is electrically connected directly with the source diffusion layer 3c, as typically shown in Fig.2.

Even if the first conductive type well (n-well) being located under the first source diffusion layer (n+ source region) and being electrically connected directly with the first drain diffusion layer (n+ drain region) would be applied to the input protection circuit shown in Fig. 7, such combination could never provide the input protection circuit of the present claims typically shown in Fig. 2.

As explained above, Becerra et al. provide no suggestion that use of the first conductive type well 1a with lower dopant concentration than the source diffusion layer 3c, which is formed directly under the source diffusion layer 3c and thereby is electrically connected directly with the source diffusion layer 3c, will be very suitable for an input/output protection circuit without any types of protective resistance element.

Applicant has amended independent claims 1, 4 and 8 to recite that the first conductive-type well is formed directly under the source diffusion layer and thereby the first conductive-type well is electrically connected directly with the source diffusion layer in conformity with the argument set forth above. As such, it is submitted that applicant's claims readily distinguish applicant's invention from the combined teachings of APA and Becerra. As such, the Patent and Trademark Office has not made out a *prima facie* case of obviousness under the provisions of 35 U.S.C. § 103.

It is submitted that the application is now in condition for allowance and an early indication of same is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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